Performance of Programmable Logic Devices (PLDs) in read-out of high speed detectors

Jack Fried

INSTRUMENTATION DIVISION

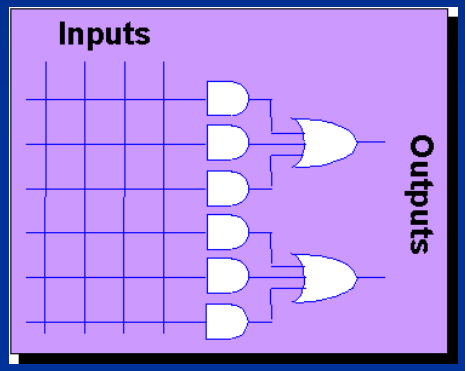
- PLD ?
- Muon Tracker PLD

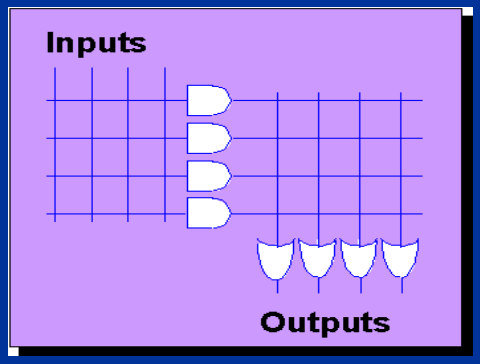
What Is a PLD

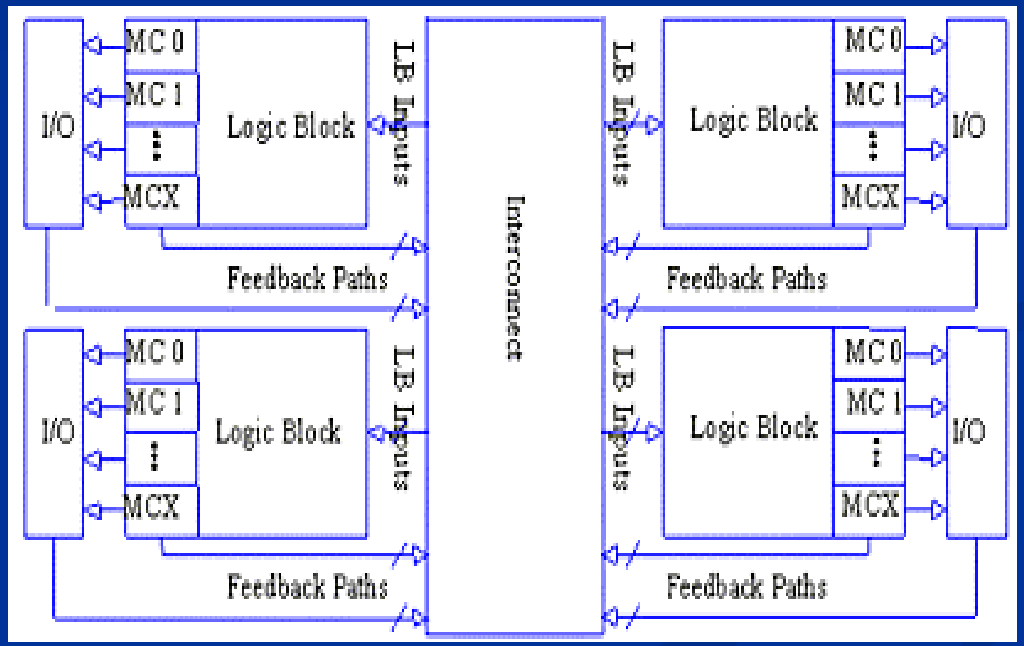
SPARTAN™
FPGA

ALTERA
APEX II

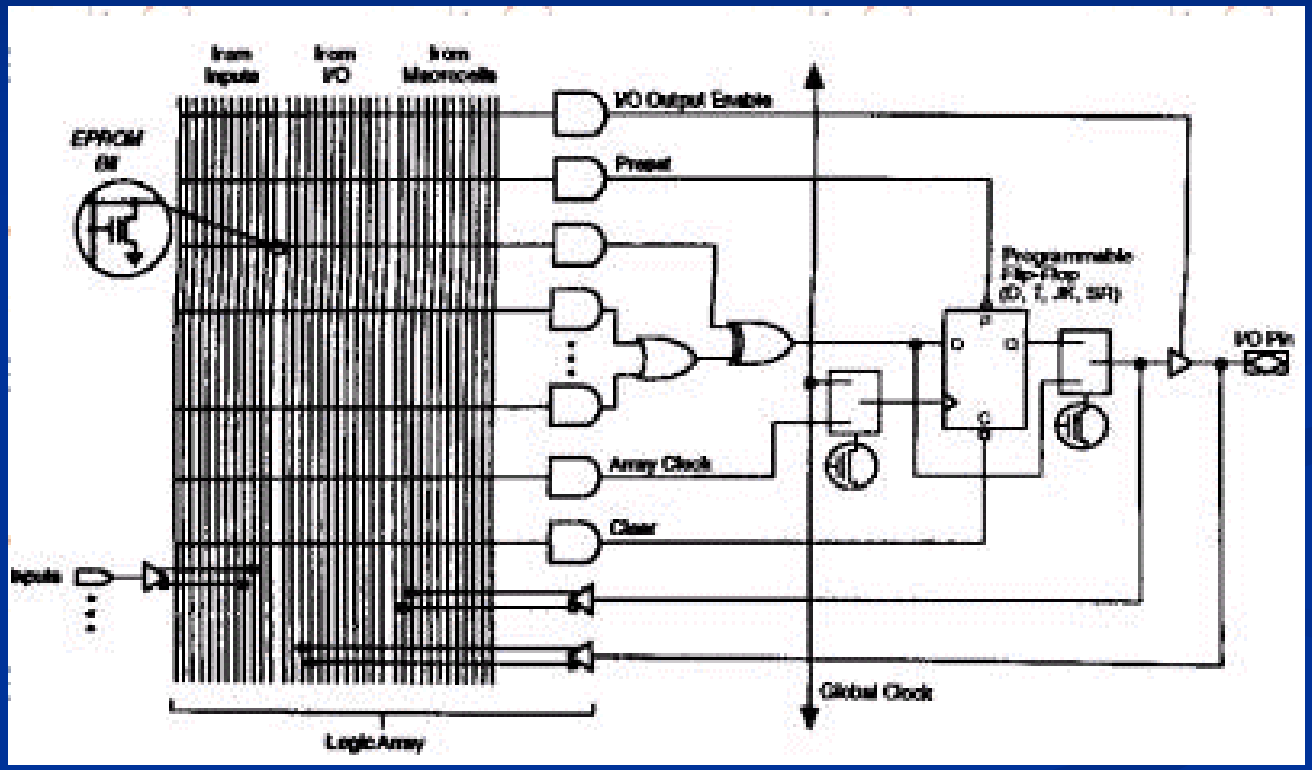
PLD Building Blocks







Logic Block


from Inputs
from I/O
from Macrocells
EPROM Bit
I/O Output Enable
Preset
Programmable Flip-Flop (D, T, JK, SR)
I/O Pin
Array Clock
Clear
Inputs
Global Clock
Logic Array

Device Features

Table 1. FLEX 10K Device Features

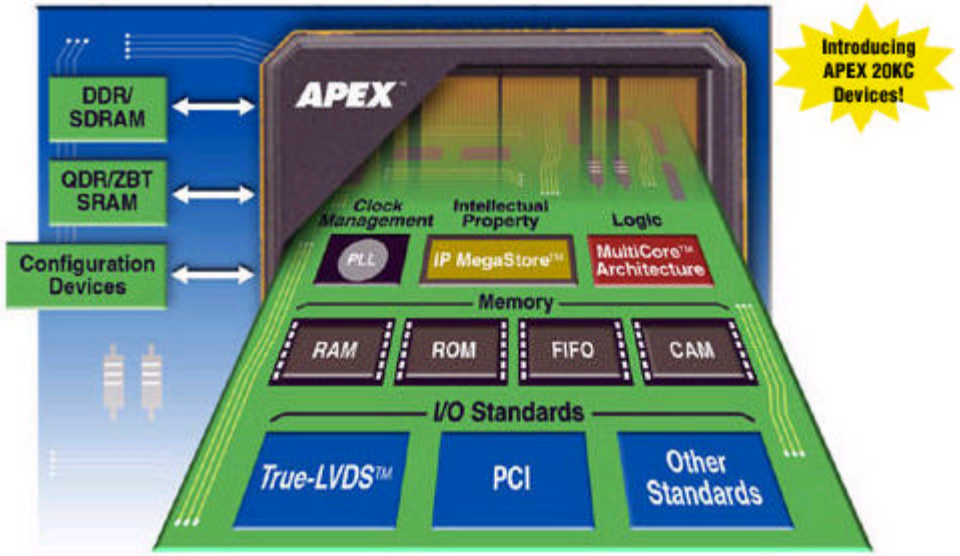
Feature	EPF10K10 EPF10K10A	EPF10K20	EPF10K30 EPF10K30A	EPF10K40	EPF10K50 EPF10K50V
Typical gates (logic and RAM) *(1)*	10,000	20,000	30,000	40,000	50,000
Maximum system gates	31,000	63,000	69,000	93,000	116,000
Logic elements (LEs)	576	1,152	1,728	2,304	2,880
Logic array blocks (LABs)	72	144	216	288	360
Embedded array blocks (EABs)	3	6	6	8	10
Total RAM bits	6,144	12,288	12,288	16,384	20,480
Maximum user I/O pins	150	189	246	189	310

Table 1. APEX II Device Features

Feature	EP2A15	EP2A25	EP2A40	EP2A70
Maximum gates	1,900,000	2,750,000	3,000,000	5,250,000
Typical gates	600,000	900,000	1,500,000	3,000,000
LEs	16,640	24,320	38,400	67,200
RAM ESBs	104	152	160	280
Maximum RAM bits	425,984	622,592	655,360	1,146,880
True-LVDS channels	36 *(1)*	36 *(1)*	36 *(1)*	36 *(1)*
Flexible-LVDS™ channels *(2)*	56	56	88	88
True-LVDS PLLs *(3)*	4	4	4	4
General-purpose PLL outputs *(4)*	8	8	8	8
Maximum user I/O pins	492	612	735	1,060

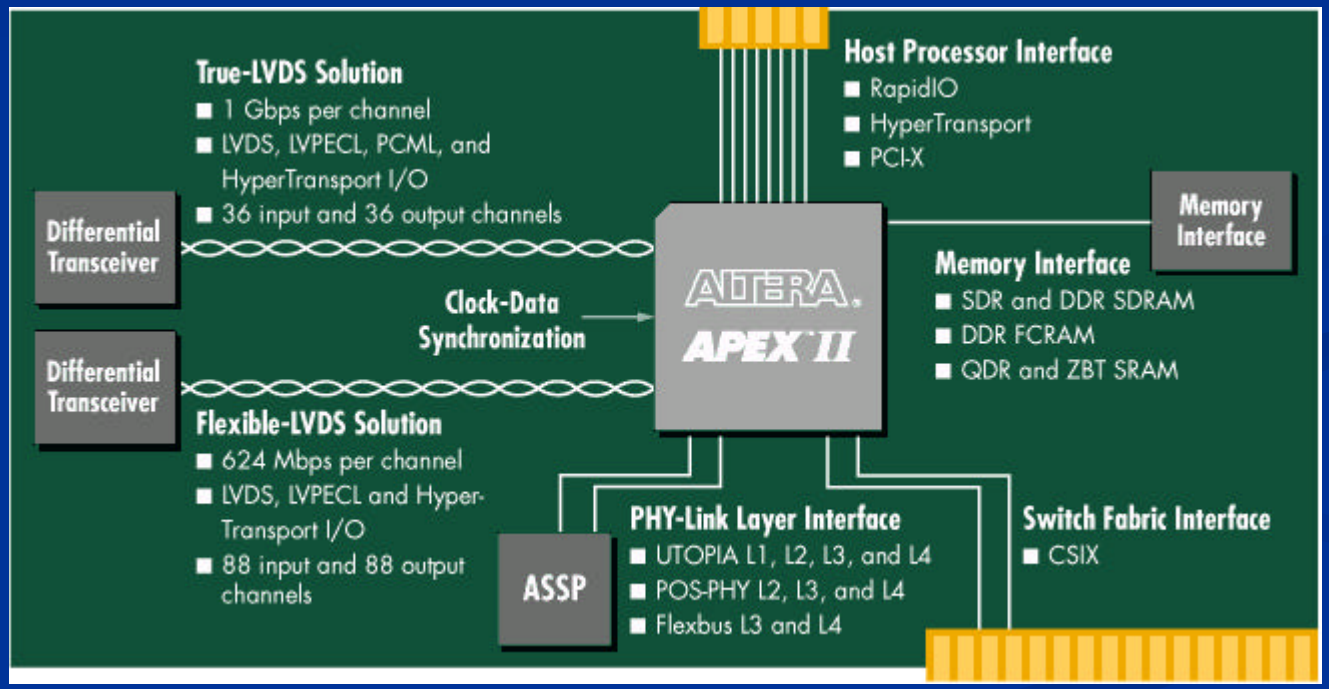
PLD Features

(cont)

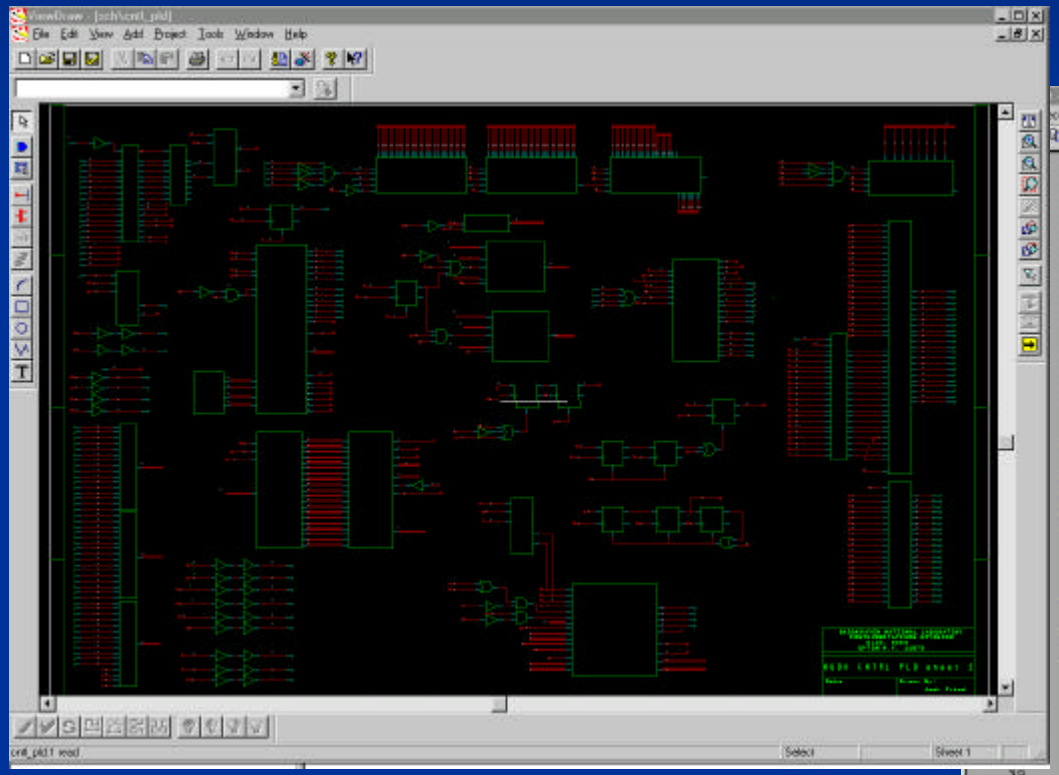


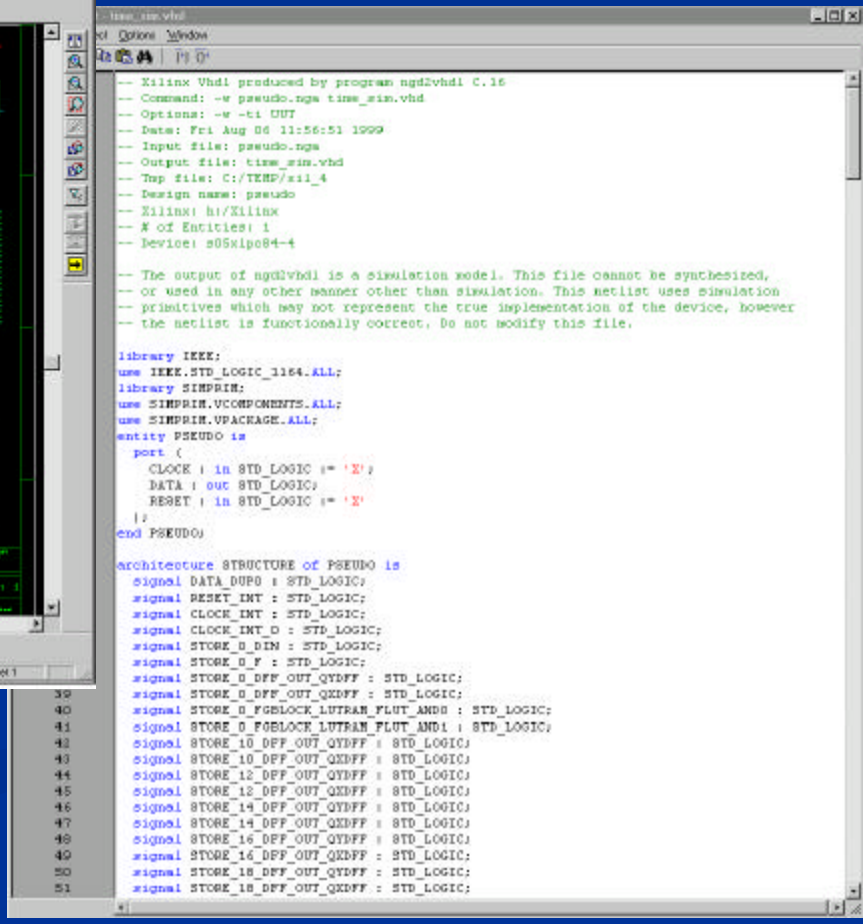
The Altera® APEX™ embedded programmable logic device (PLD) family, meets the system-level design challenge by offering complete system integration on a single device.
(Click on the features above for more information.)

I/O Protocols



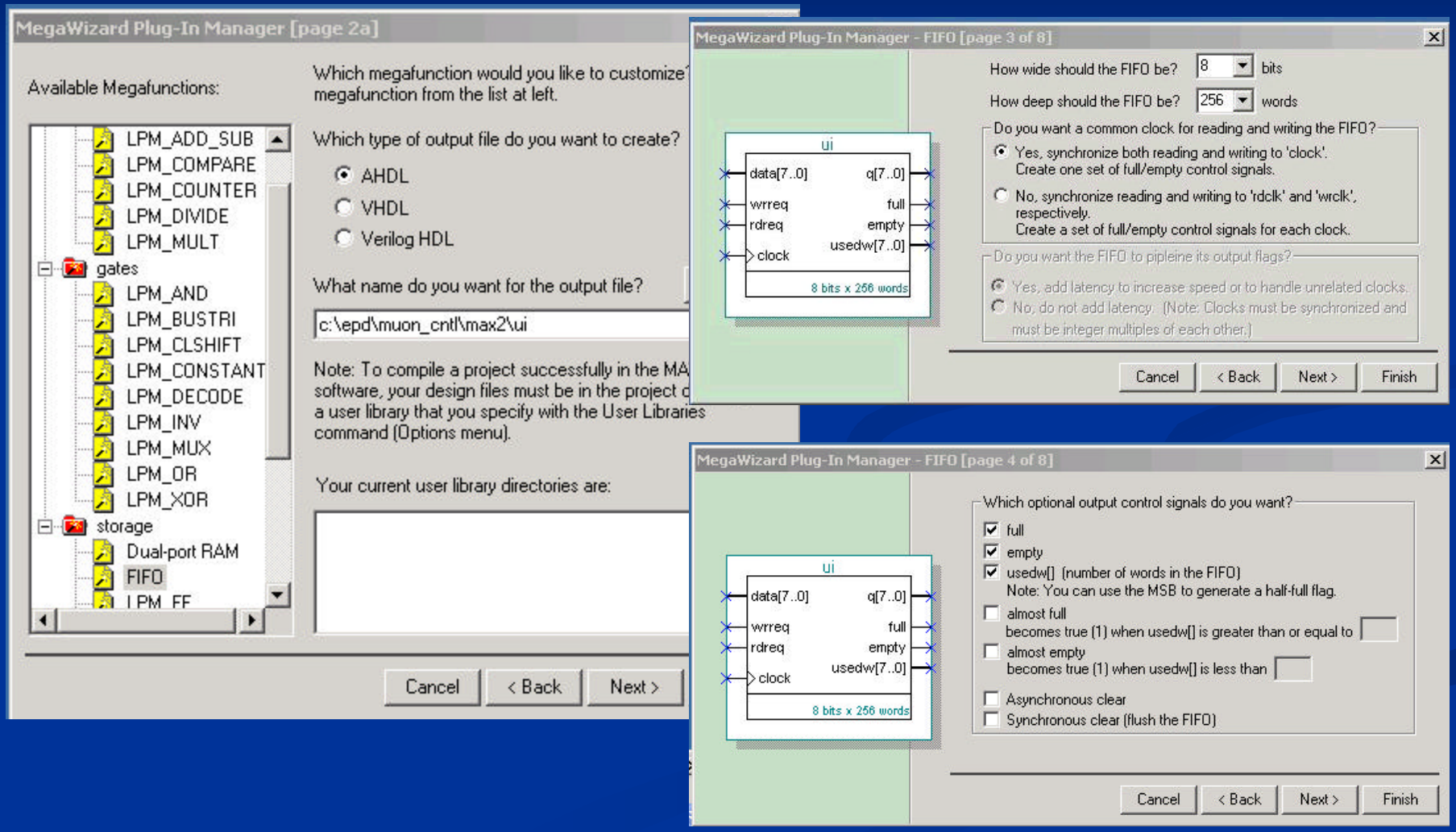
Design Entry





```
-- Xilinx Vhdl produced by program ngd2vhdl C.16
-- Command: -w pseudo.ngm time_sim.vhd
-- Options: -w -ti UUT
-- Date: Fri Aug 06 11:56:51 1999
-- Input file: pseudo.ngm
-- Output file: time_sim.vhd
-- Tmp file: C:/TEMP/xil_4
-- Design name: pseudo
-- Xilinx: h:/Xilinx
-- # of Entities: 1
-- Device: s05xlpq84-4

-- The output of ngd2vhdl is a simulation model. This file cannot be synthesized,
-- or used in any other manner other than simulation. This netlist uses simulation
-- primitives which may not represent the true implementation of the device, however
-- the netlist is functionally correct. Do not modify this file.

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
library SIMPRIM;
use SIMPRIM.VCOMPONENTS.ALL;
use SIMPRIM.VPACKAGE.ALL;
entity PSEUDO is
  port (
    CLOCK : in STD_LOGIC := 'X';
    DATA : out STD_LOGIC;
    RESET : in STD_LOGIC := 'X'
  );
end PSEUDO;

architecture STRUCTURE of PSEUDO is
  signal DATA_DUPO : STD_LOGIC;
  signal RESET_INT : STD_LOGIC;
  signal CLOCK_INT : STD_LOGIC;
  signal CLOCK_INT_O : STD_LOGIC;
  signal STORE_0_DIN : STD_LOGIC;
  signal STORE_0_F : STD_LOGIC;
  signal STORE_0_DFF_OUT_QYDFF : STD_LOGIC;
  signal STORE_0_DFF_OUT_QXDFF : STD_LOGIC;
  signal STORE_0_FGBLOCK_LUTRAM_FLUT_AND0 : STD_LOGIC;
  signal STORE_0_FGBLOCK_LUTRAM_FLUT_AND1 : STD_LOGIC;
  signal STORE_10_DFF_OUT_QYDFF : STD_LOGIC;
  signal STORE_10_DFF_OUT_QXDFF : STD_LOGIC;
  signal STORE_12_DFF_OUT_QYDFF : STD_LOGIC;
  signal STORE_12_DFF_OUT_QXDFF : STD_LOGIC;
  signal STORE_14_DFF_OUT_QYDFF : STD_LOGIC;
  signal STORE_14_DFF_OUT_QXDFF : STD_LOGIC;
  signal STORE_16_DFF_OUT_QYDFF : STD_LOGIC;
  signal STORE_16_DFF_OUT_QXDFF : STD_LOGIC;
  signal STORE_18_DFF_OUT_QYDFF : STD_LOGIC;
  signal STORE_18_DFF_OUT_QXDFF : STD_LOGIC;
```

Plug In Manager

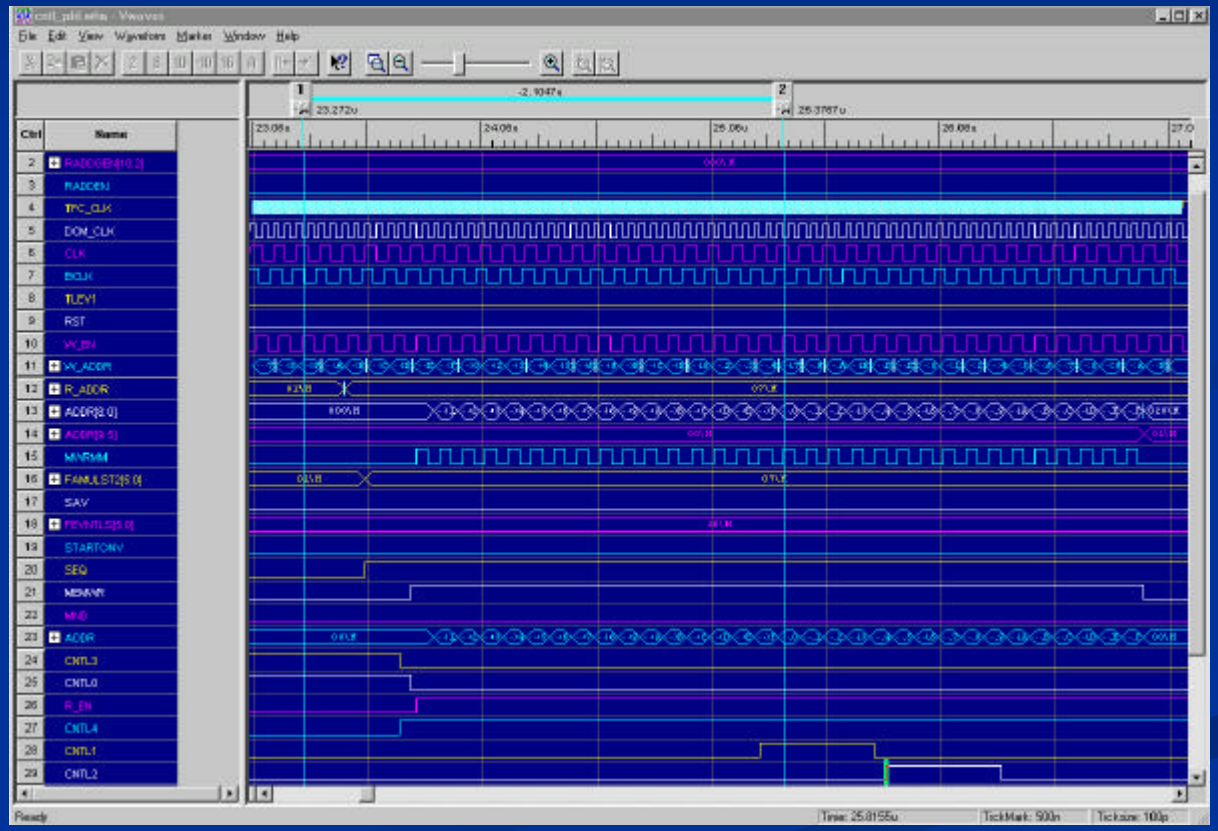


Mega Functions

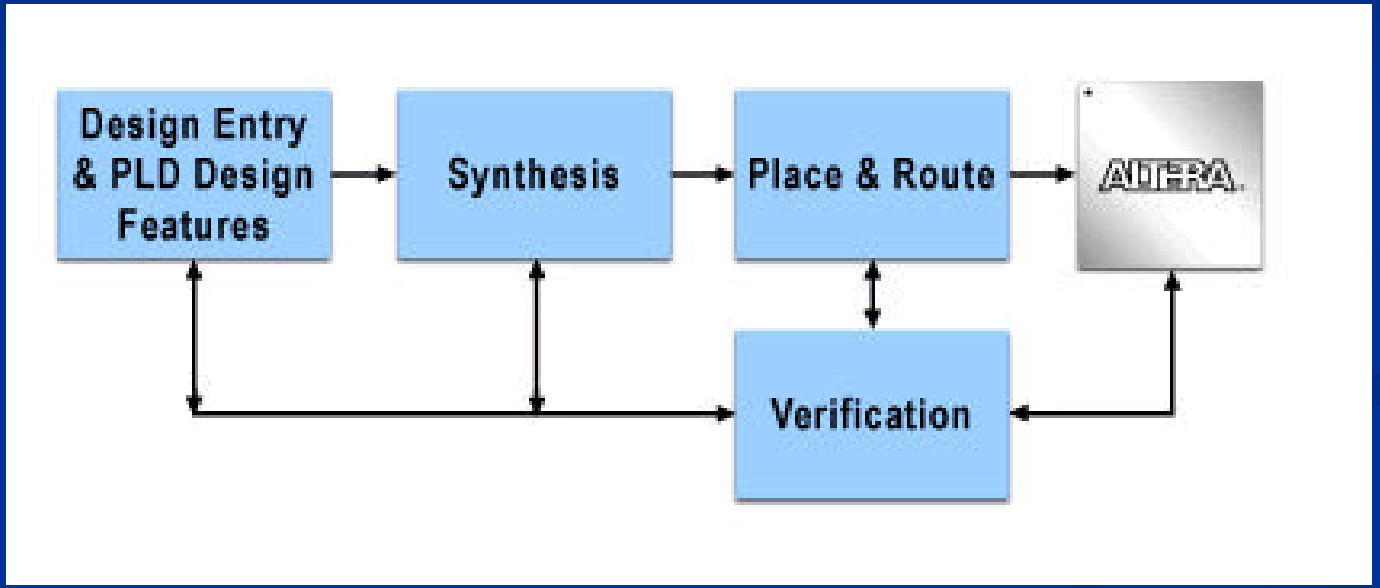
Megafunction Name *Vendor*	PDF	Free Evaluation	Certifications	Device Familes Supported
10/100 Ethernet MAC *Altera Corporation*		Try OpenCore	SOPC Builder Ready, I-Tested	APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, HardCopy
8b10b Encoder/Decoder version 1.1.0 *Altera Corporation*		Try OpenCore		ACEX, FLEX 10KE, APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, Mercury, HardCopy
ARM922T *Altera Corporation*			SOPC Builder Ready	ARM-based Excalibur
ATM Cell Processor Compiler *Altera Corporation*		Try OpenCore	Atlantic Compliant	APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, HardCopy
Avalon DMA *Altera Corporation*			SOPC Builder Ready	FLEX 10KE, ACEX 1K, APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, Stratix, HardCopy
Avalon Interface to User Logic *Altera Corporation*			SOPC Builder Ready	FLEX 10KE, ACEX 1K, APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, Stratix, HardCopy
Avalon On-Chip RAM *Altera Corporation*			SOPC Builder Ready	FLEX 10KE, ACEX 1K, APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, Stratix, HardCopy
Avalon On-Chip ROM *Altera Corporation*			SOPC Builder Ready	FLEX 10KE, ACEX 1K, APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, Stratix, HardCopy
Avalon PIO *Altera Corporation*			SOPC Builder Ready	FLEX 10KE, ACEX 1K, APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, Stratix, HardCopy
Avalon SDRAM Controller *Altera Corporation*			SOPC Builder Ready	FLEX 10KE, ACEX 1K, APEX 20KE, APEX 20KC, APEX II, ARM-based Excalibur, Stratix, HardCopy

Design Verification

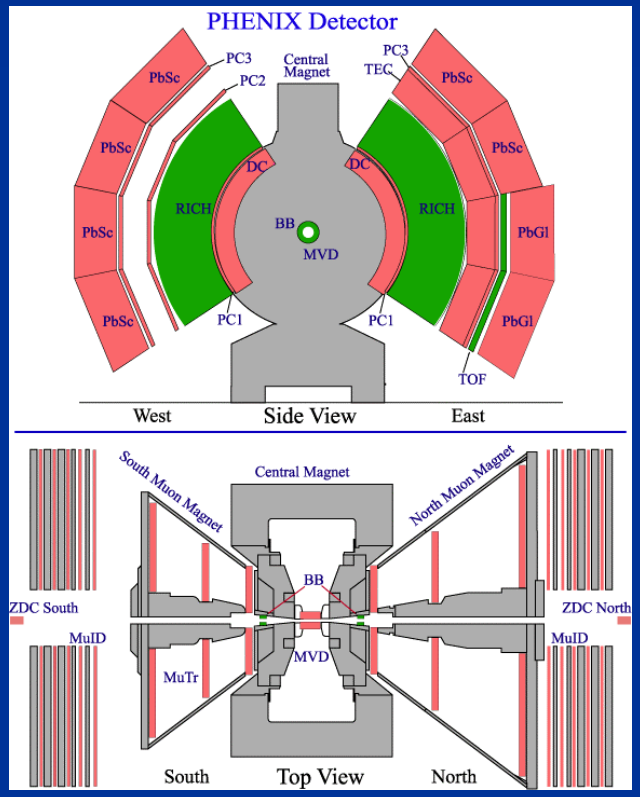
- Simulation
- Built in real time Logic analyzer

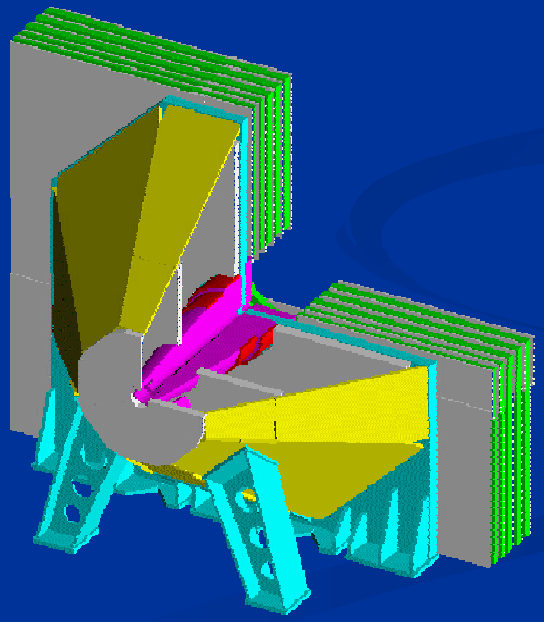


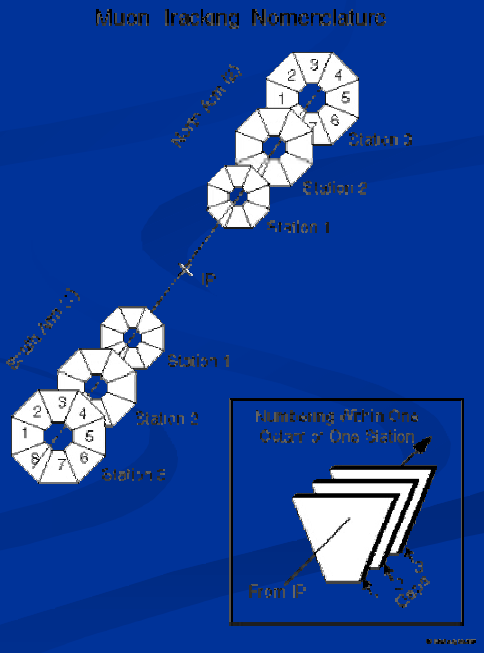
PLD Design Flow



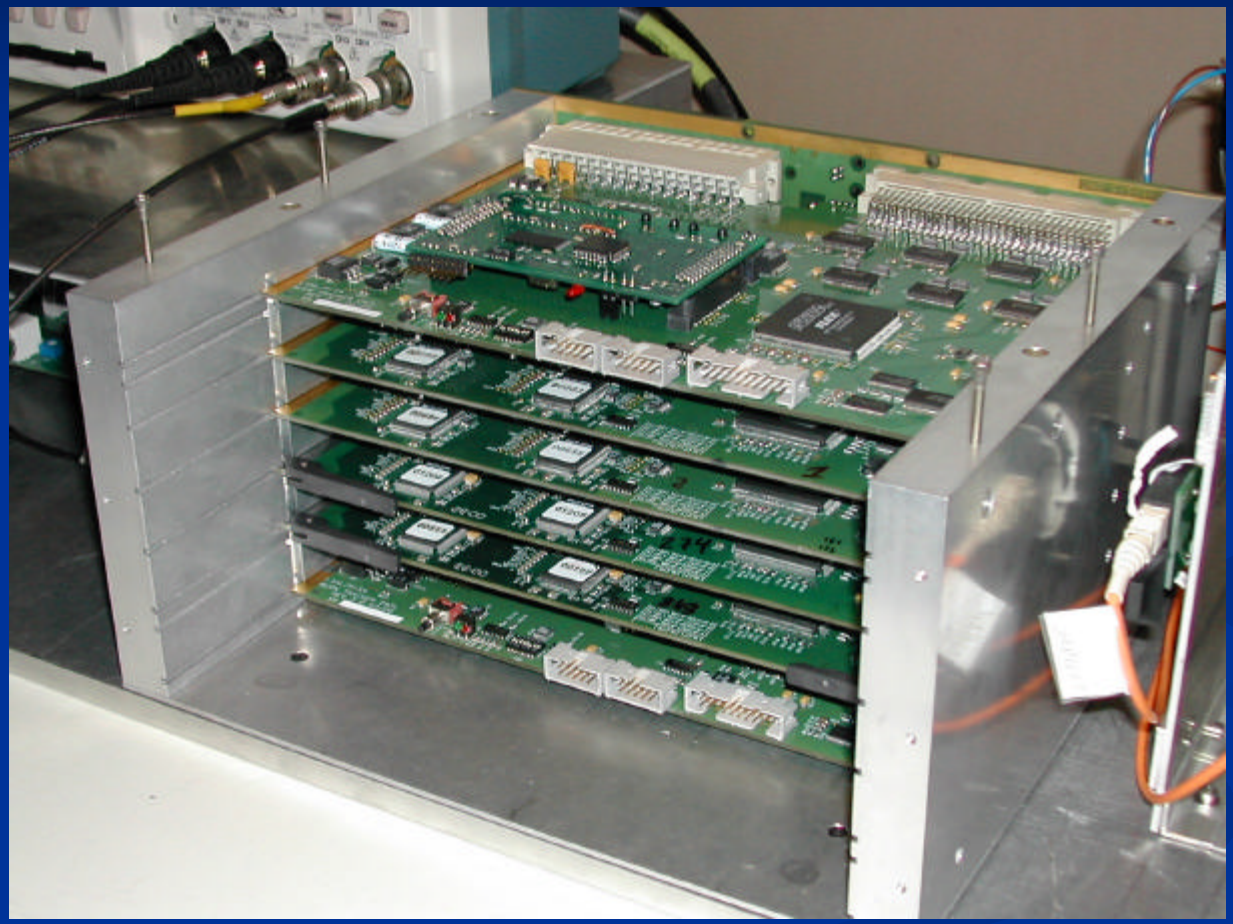
PHENIX Muon Tracker





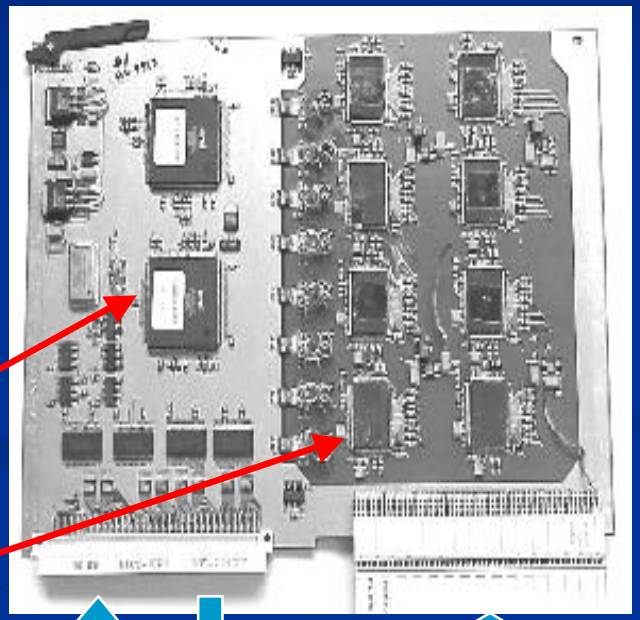


Muon Tracker Crate



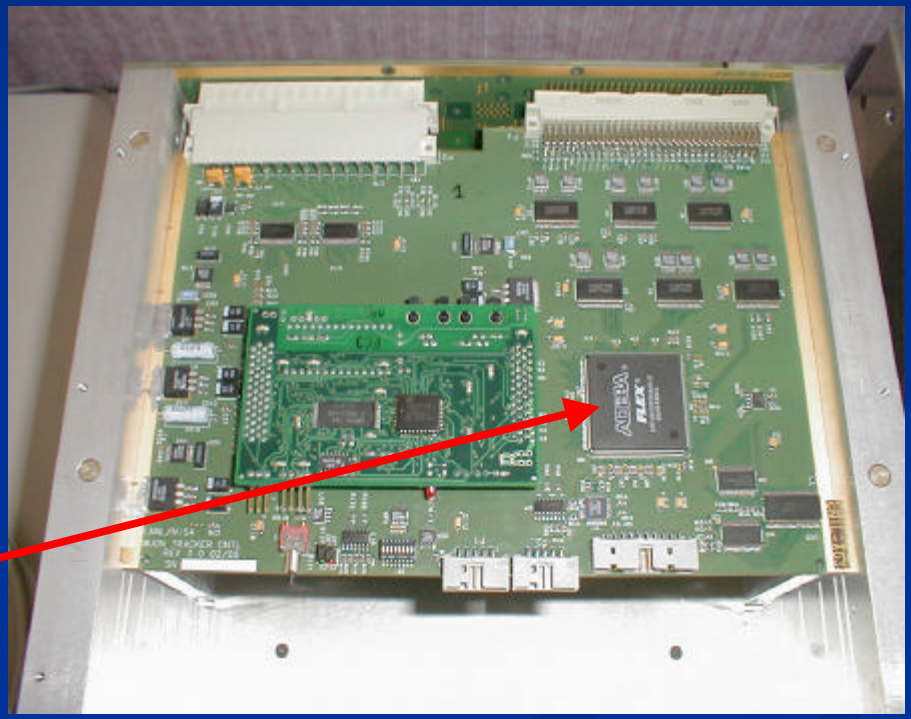
Cathodes Read-Out Card (CROC)

- Design Requirements
  - 64 Channel Readout per CROC
  - Less than 3125 electrons (RMS) noise for 10-150 pF of detector capacitance (including 24” cable) •
  - Less than 1% crosstalk between any channels on the board
  - gain: 3.5mV/fC
  - Digital/Analog isolation
- Main Components
  - AMU-ADC
  - CPA



Controller Card (CNTL)

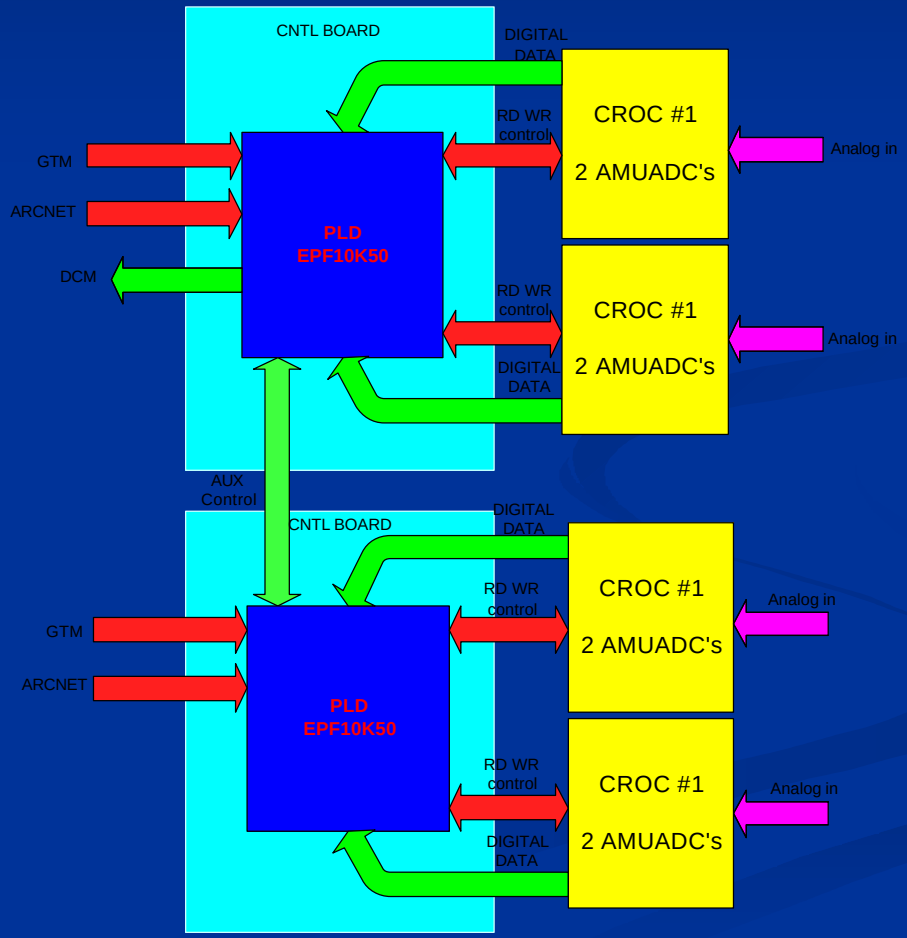
- Design Requirements
  - Control AMU/ADC data collection, conversion and read-out
  - Provide connection to 2 CROC boards
  - Provide connection to the outside world
  - Support the T&FC and DCM interface
  - Provide data relay from remote controller board to DCM
  - Support ARCnet connectivity to serial configuration bus
- FPGA - the brain
  - developed by Jack
  - work in progress



CNTL Card

Muon Tracker Crate

Block Diagram



Requirements for Muon tracker PLD

- Trigger rate 25Khz
- 4 samples per pulse
- Sample new data on every beam crossing
- Holds 5 events
- 100ns between triggers (burst rate)
- Control digital part of AMUADC -RD-WR
- Send data to DCM
- Allow for Master and slave modes

Muon Tracker
PLD Programming Difficulties

- Board already designed
  - PLD already chosen (FLEX10K50E)
  - Pins allocated
  - PLD to small
- Overlapping events
- AMUADC noise problems
- AMUADC requires special RD WR sequence

ALTERA
10K50

Table 1. FLEX 10KE Device Features

Feature	EPF10K30E	EPF10K50E EPF10K50S
Typical gates *(1)*	30,000	50,000
Maximum system gates	119,000	199,000
Logic elements (LEs)	1,728	2,880
EABs	6	10
Total RAM bits	24,576	40,960
Maximum user I/O pins	220	254

Figure 1. FLEX 10KE Device Block Diagram

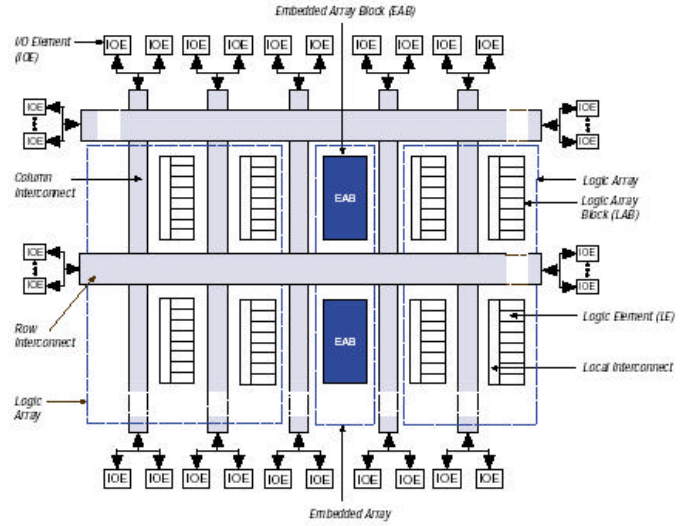


Figure 5. FLEX 10KE EAB Memory Configurations

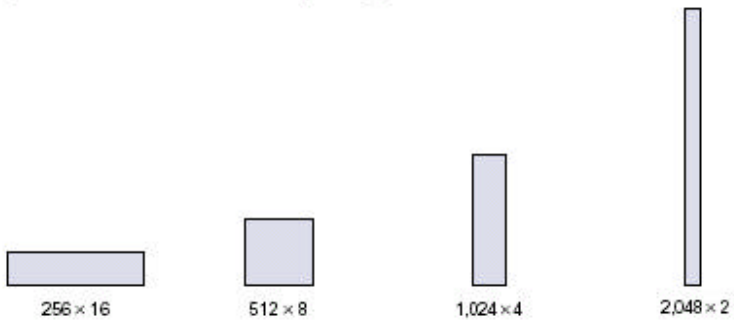
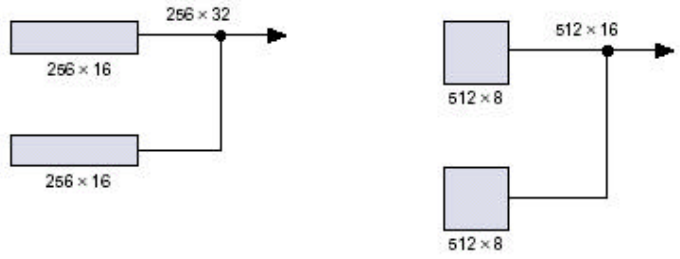


Figure 6. Examples of Combining FLEX 10KE EABs



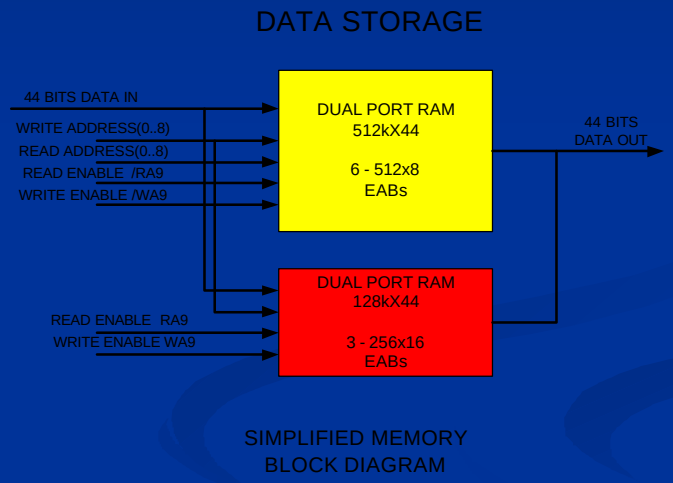
Memory Requirements

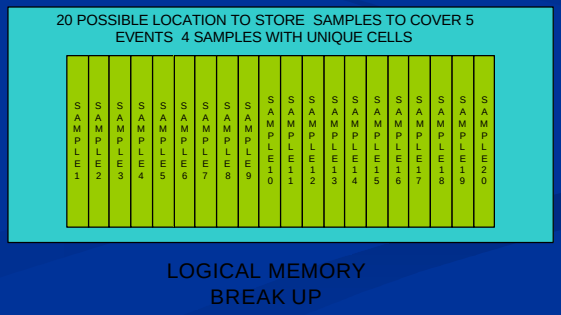
- 4 samples per event
- Need to be able to store 5 events
- Each sample is 11bits
- 32 channels per AMUADC
  - 4 AMUADC PER CNTL 128 channels

28160 BITS TOTAL

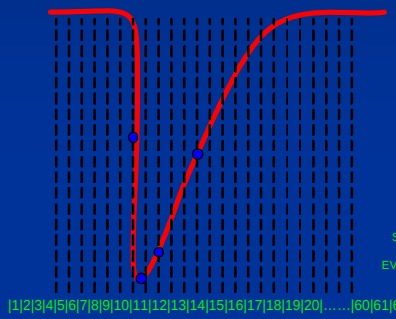
Memory Implementation

- Used 9 EABs
- Only 1 EAB left for PLD algorithm
- Lost 8704 bits





AMUADC cell Writing & Reading



|1|2|3|4|5|6|7|8|9|10|11|12|13|14|15|16|17|18|19|20|……|60|61|62|63|64|

40 beam clocks back

TRIGGER LVL1

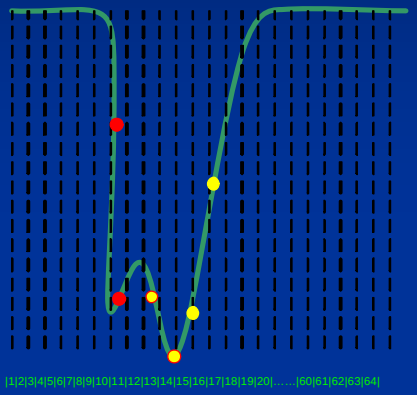
|1|2|3|4|5|6|7|8|9|10|11|12|13|14|15|16|17|18|19|20|……|60|61|62|63|64|

SAMPLES 10 11 12 15

|1|2|3|4|5|6|7|8|9|13|14|16|17|18|19|20|……|60|61|62|63|64|

AFTER CELLS SELECTED THEY ARE REMOVED TILL CONVERTED AND STORED THEN THEY ARE PUT BACK

Overlapping Events



OVERLAPPING EVENT

STORES ANALOG VALUE EVERY BEAM CLOCK

|1|2|3|4|5|6|7|8|9|10|11|12|13|14|15|16|17|18|19|20|……|60|61|62|63|64|

TRIGGER LVL1

4 CLOCK LATER

40 beam clocks back

|1|2|3|4|5|6|7|8|9|10|11|12|13|14|15|16|17|18|19|20|……|60|61|62|63|64|

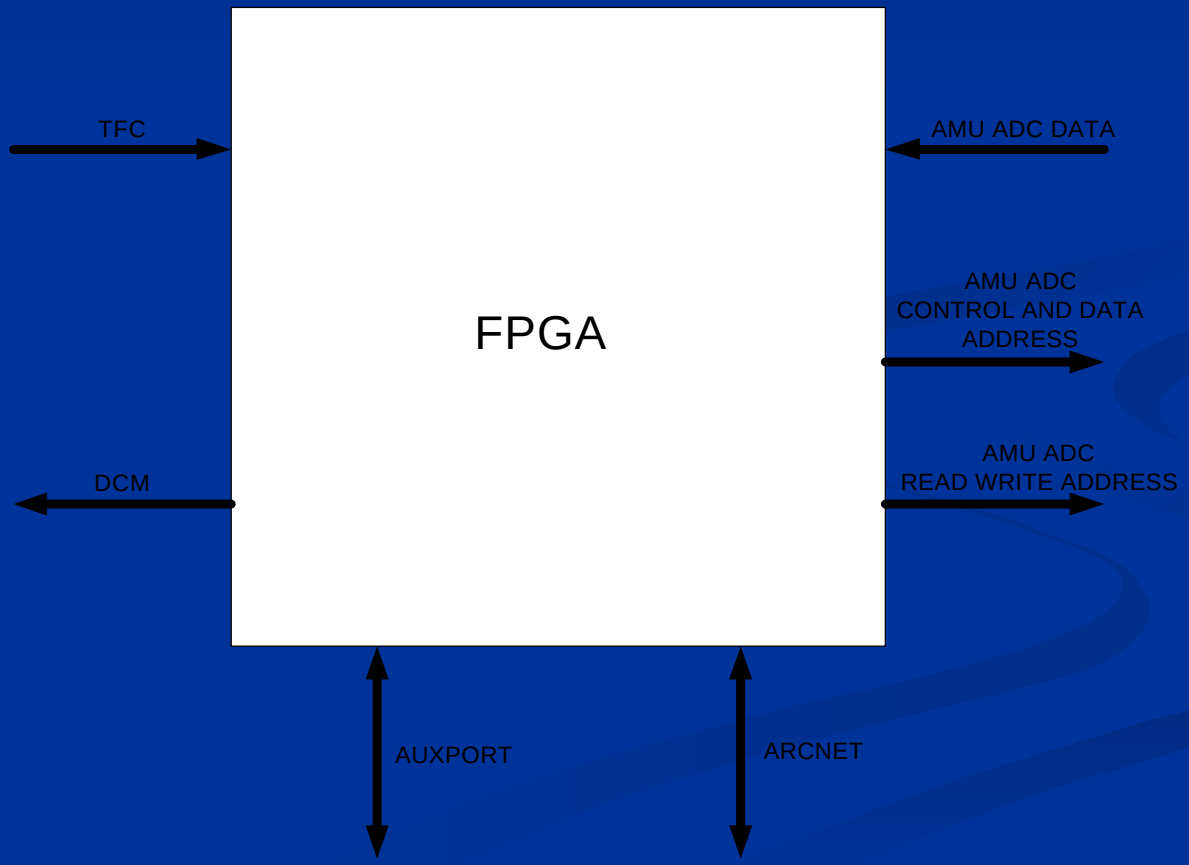
SAMPLES 10 11 13 15

SAMPLES 14 15 17 19

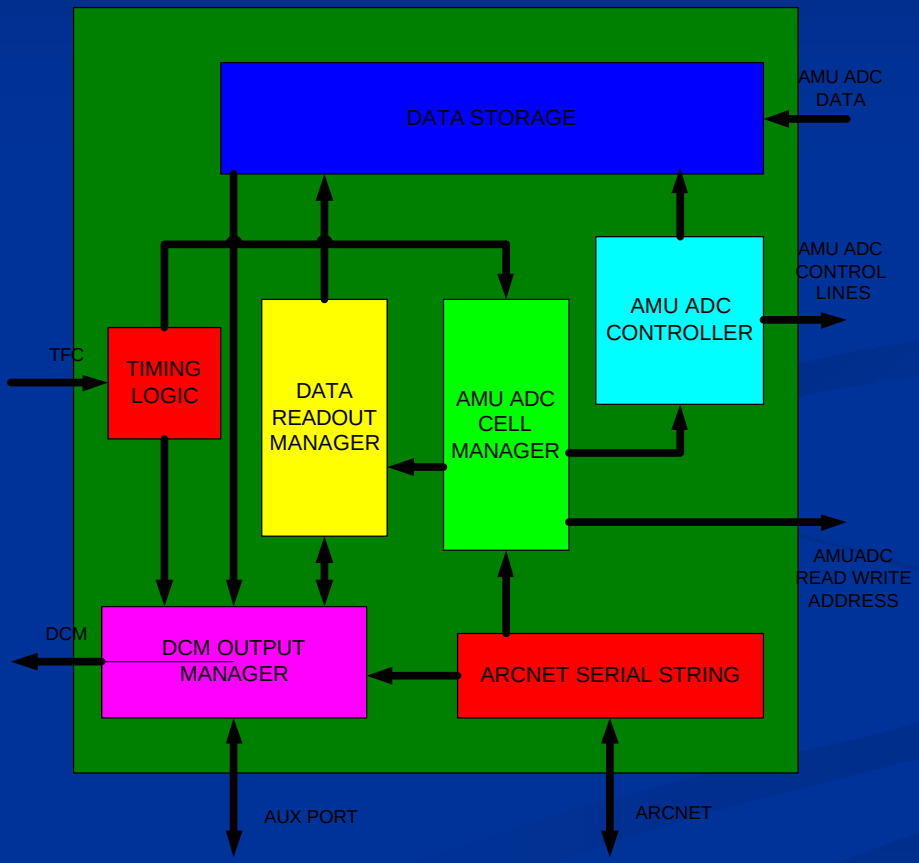
|1|2|3|4|5|6|7|8|9|12|16|18|20|……|60|61|62|63|64|

AFTER CELLS SELECTED THEY ARE REMOVED TILL CONVERTED AND STORED THEN THEY ARE PUT BACK

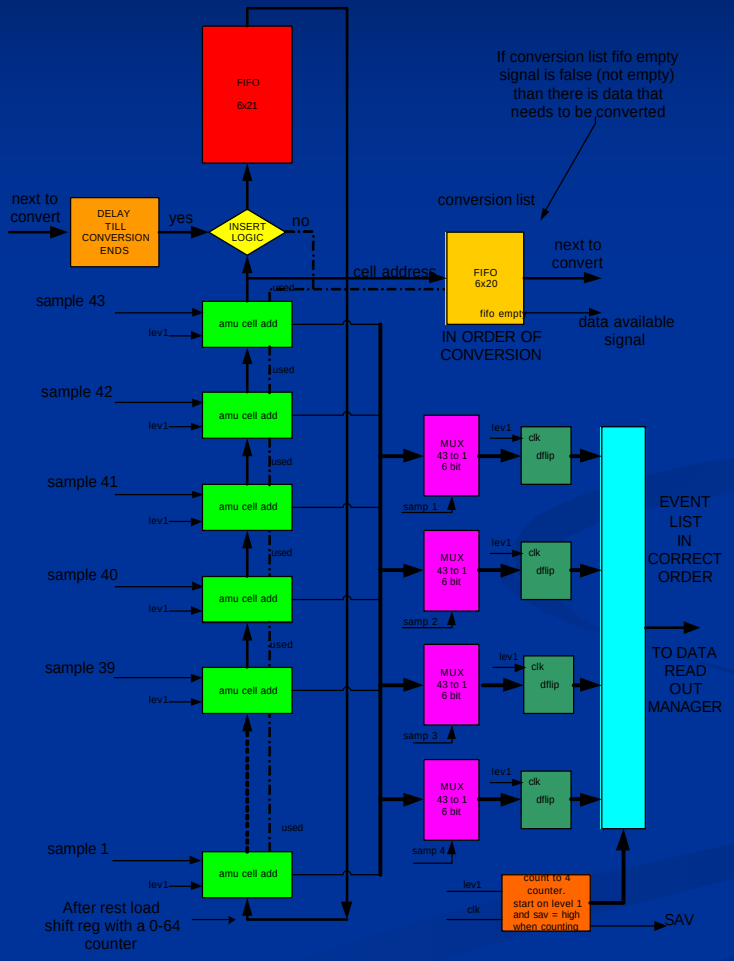
MUON TRACKER PLD



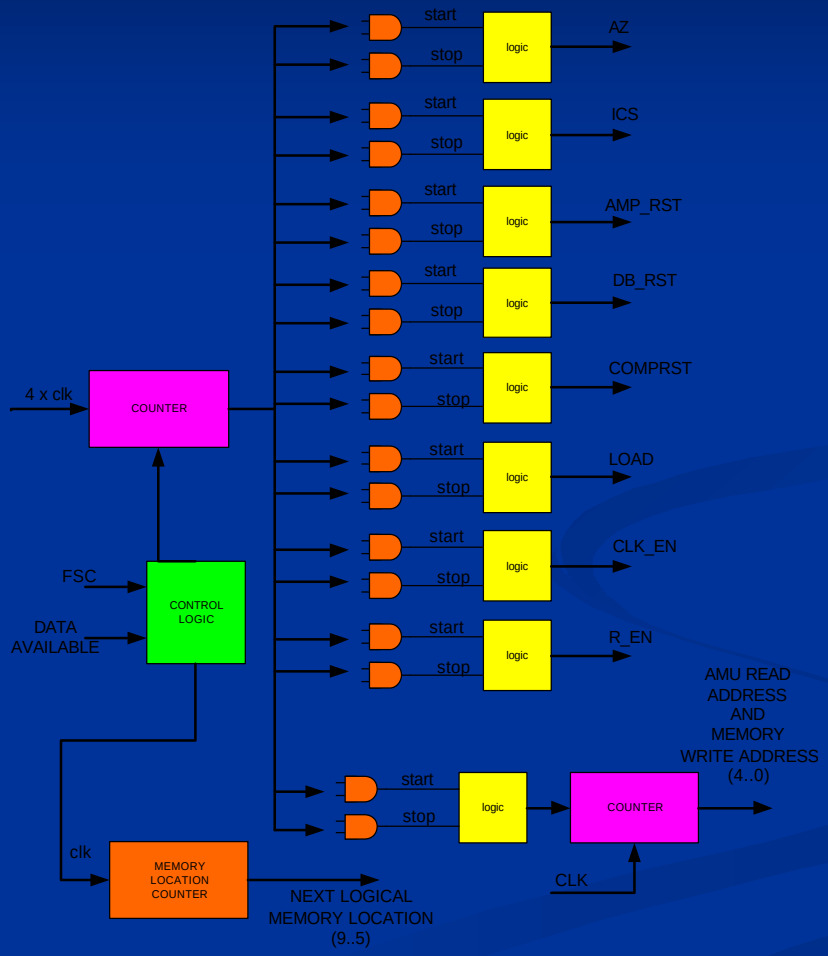
MUON TRACKER PLD



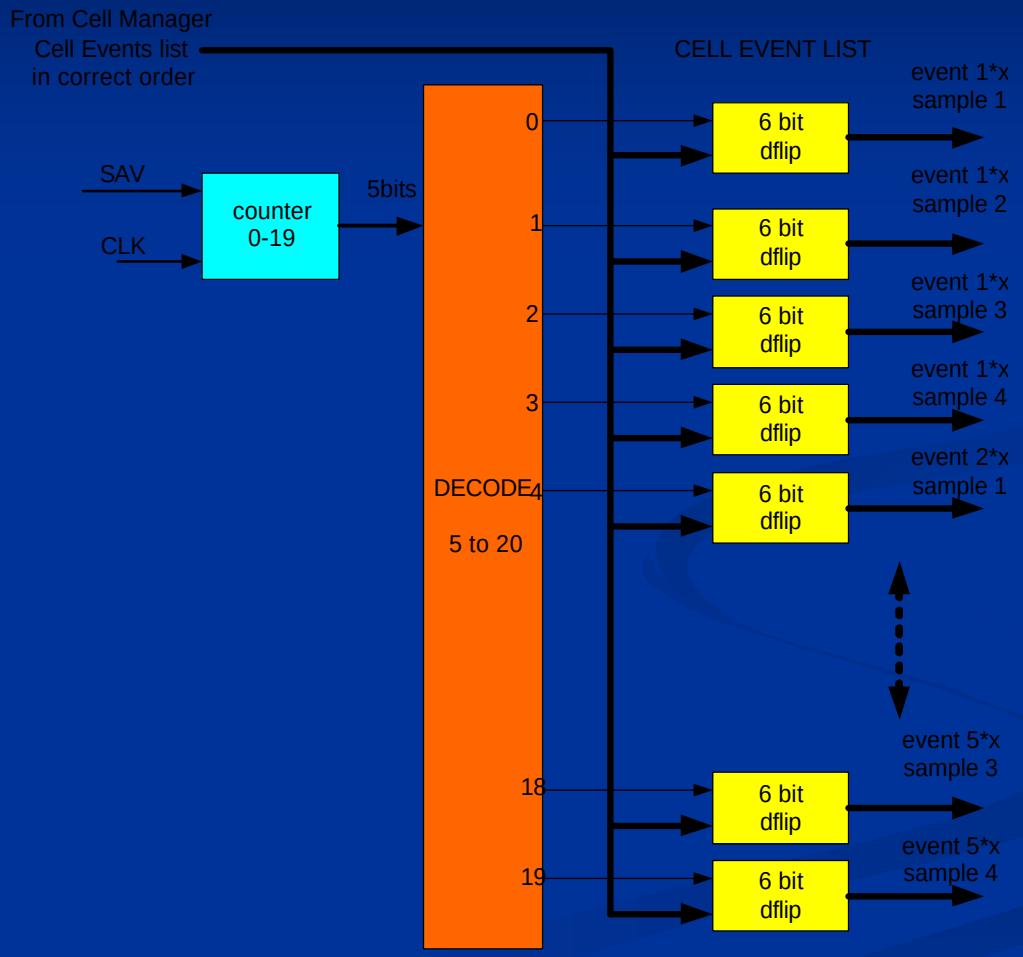
AMU Cell Manager



AMUADC Controller



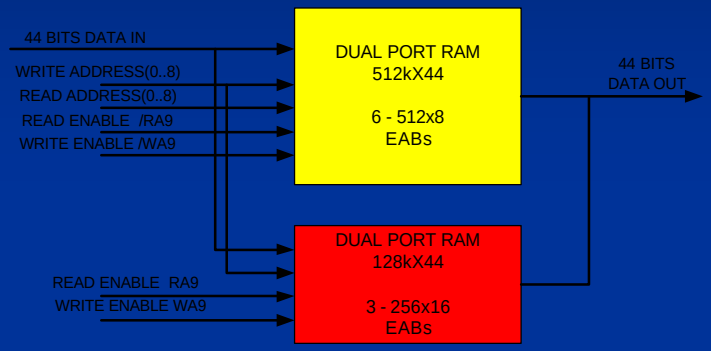
Read Out Manager part1



Read Out Manager part2

Read Out Manager Part3

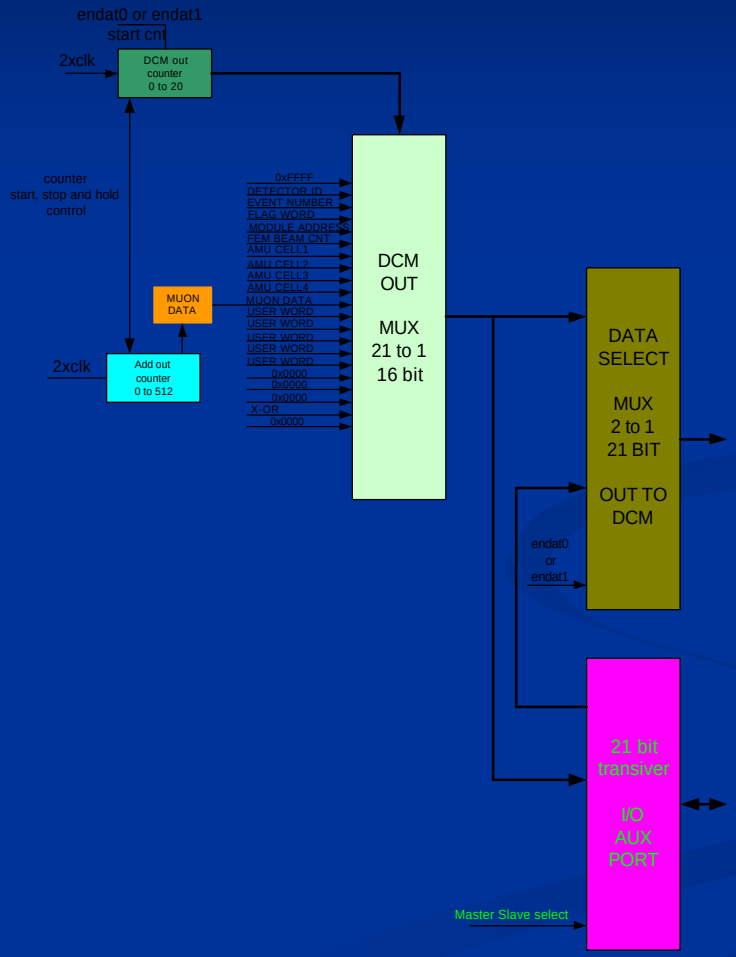
DATA STORAGE



SIMPLIFIED MEMORY
BLOCK DIAGRAM

LOGICAL MEMORY
BREAK UP

DCM Output Manager

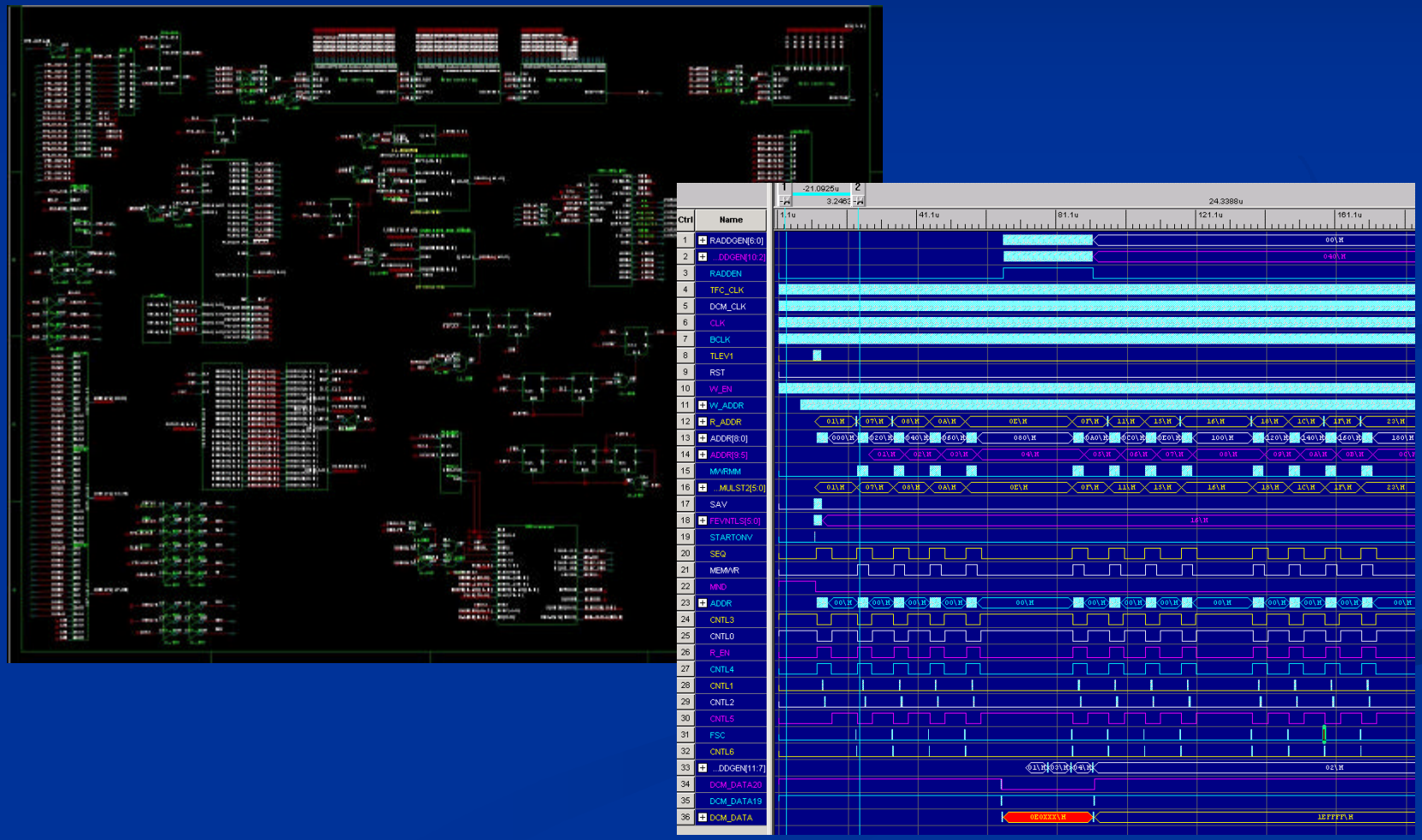


Compilation Result

```
***** Project compilation was successful



** DEVICE SUMMARY **

Chip/                                Input Output Bidir  Memory  Memory                    LCs
POF      Device                      Pins  Pins   Pins   Bits %  Utilized  LCs  % Utilized

cntl_pld EPF10K50EQI240-2 81     68     20   28352     69 %    2403     83 %

User Pins:                 81     68     20
```

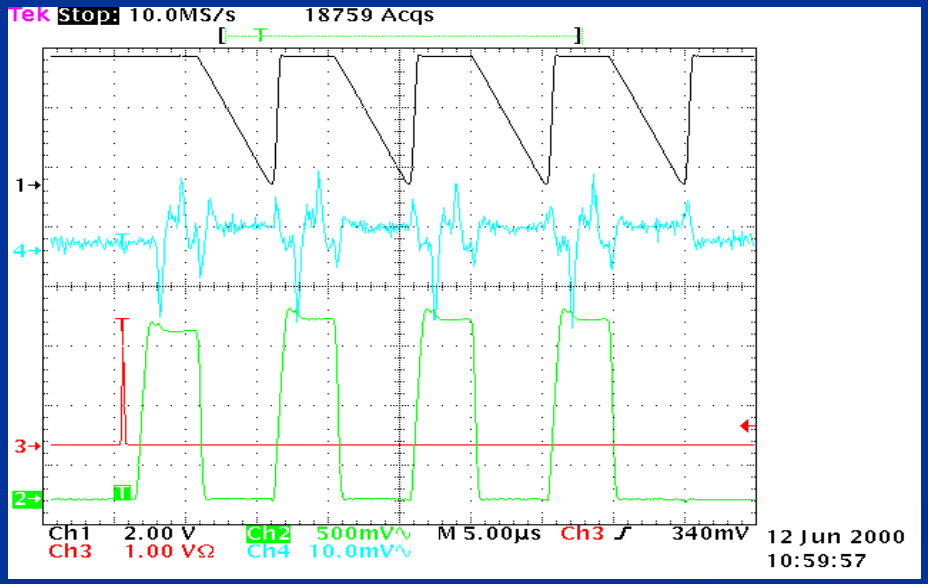
```
Total dedicated input pins used:                3/6       (  50%)
Total I/O pins used:                          166/183     (  90%)
Total logic cells used:                      2403/2880    (  83%)
Total embedded cells used:                     94/160     (  58%)
Total EABs used:                               10/10      ( 100%)
Average fan-in:                                2.16/4     (  54%)
Total fan-in:                                4238/11520   (  36%)

Total input pins required:                      81
Total input I/O cell registers required:        20
Total output pins required:                     68
Total output I/O cell registers required:        3
Total buried I/O cell registers required:        0
Total bidirectional pins required:              20
Total reserved pins required                     0
Total logic cells required:                   2403
Total flipflops required:                     1141
Total packed registers required:                 0
Total logic cells in carry chains:             142
Total number of carry chains:                   22
Total number of carry chains of length  1-8 :   19
Total number of carry chains of length  9-16:    3
Total logic cells in cascade chains:           532
Total number of cascade chains:                265
Total single-pin Clock Enables required:         0
Total single-pin Output Enables required:        0
Logic cells inserted for fitting:               27

Synthesized logic cells:                      159/2880     (   5%)
```

Current code



Muon FEE

- PLD - current code
  - store every beam crossing
  - 4-sample per pulse
  - readout time 53uS
  - hold 4 events



Time

END